IN THE CLAIMS

Please amend the claims as indicated below.

Claims 1-10 cancelled.

Claims 11-14 cancelled.

15. (Currently Amended) The integrated circuit of claim ~~14~~23, wherein said immunity enable signal is generated dynamically or is fixed during manufacture of said integrated circuit.

Claim 16 (Cancelled).

17. (Currently Amended) The integrated circuit of claim ~~16~~24, wherein said immunity enable signal is generated dynamically or is fixed during manufacture of said integrated circuit.

Claims 18-20 cancelled.

Please add the following new claims.

21. (New) An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; and

a keeper circuit capable of alternating the soft error susceptibility of said dynamic logic gate, the keeper circuit providing a selectable critical charge to the output node, the keeper circuit coupled to the output node and coupled to a feedback device, the keeper circuit and a precharge

device of the dynamic logic gate coupled to an output of a multiplexer, the multiplexer adapted to selectively couple the keeper circuit and the precharge device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of the multiplexer.

22. (New) An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected;

a keeper circuit capable of altering the soft error susceptibility of said dynamic logic gate, the keeper circuit providing a selectable critical charge to the output node, the keeper circuit coupled to the output node of a first multiplexer adapted to selectively couple the keeper circuit to one of two or more voltage supplies in response to an immunity enable signal received on a control input of the first multiplexer; and

a second multiplexer adapted to selectively couple a precharge device of the dynamic logic gate to the same voltage supply that the keeper circuit is coupled to, in response to an immunity enable signal received on a control input of the second multiplexer.

23. (New) An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected;

a selectable circuit capable of alternating the soft error susceptibility of said dynamic logic gate;

a keeper circuit providing a critical charge to the output node, the keeper circuit coupled to the output node and coupled to a feedback device; and

a body bias circuit, the body bias circuit adapted to selectively alter the susceptibility of input devices of the dynamic logic gate to radiation events, the body bias circuit including a multiplexer adapted to selectively couple the bodies of the input devices to one of two or more biasing voltages in response to an immunity enable signal received on a control input of the multiplexer.

24. (New) An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; and

a keeper circuit adapted to selectively alter the critical charge of the dynamic logic gate, the keeper circuit providing a selectable critical charge to the output node, the keeper device coupled to the output node and coupled to a feedback device, the keeper circuit and a precharge device of the dynamic logic gate coupled to an output of a multiplexer, the multiplexer adapted to selectively couple the keeper device and the precharge device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of the multiplexer.

25 (New) An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected;

a keeper circuit adapted to selectively alter the critical charge of the dynamic logic gate, the keeper circuit including:

a keeper device providing a selectable critical charge to the output node, the keeper device coupled to the output node and coupled to a feedback device, the keeper

device coupled to an output of a first multiplexer adapted to selectively couple the keeper device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of the first multiplexer; and

a second multiplexer adapted to selectively couple a precharge device of the dynamic logic gate to the same voltage supply that the keeper device is coupled to in response to an immunity enable signal received on a control input of the second multiplexer.

26. (New) An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected;

a keeper circuit providing a level of critical charge to the output node, a keeper device coupled to the output node and coupled to a feedback device; and

a body bias circuit, the body bias circuit adapted to selectively alter the bias voltage applied to the bodies of input devices of the dynamic logic gate, the body bias circuit including a multiplexer adapted to selectively couple the bodies of the input devices of the dynamic logic gate to one of two or more biasing voltages in response to an immunity enable signal received on a control input of the multiplexer.

REJECTION OF CLAIMS 1-6, 9, 11-13, 18 AND 19 UNDER 35 U.S.C. SECTION 102

The Examiner rejected claims 1-6, 9, 11-13, 18 and 19 under 35 U.S.C. Section 102 (b) and (e). Claims 1-6, 9 11-13, 18 and 19 have been cancelled.

ALLOWABLE SUBJECT MATTER

The Examiner stated that claims 7-8, 10, 14-17, and 20 would be allowable if rewritten in independent form to include all of the limitations of any base claim and any intervening claims. Claims 7, 8, 10, 14, 16, and 20 have been rewritten in such form as new claims 21, 22, 23, 24, 25, and 26, respectively.

SUMMARY AND CONCLUSION

In view of the foregoing, withdrawal of the rejections and the allowance of the current pending claims is respectfully requested. If the Examiner feels that the pending claims could be allowed with minor changes, the Examiner is invited to telephone the undersigned to discuss an Examiner's Amendment.

Respectfully submitted,

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